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A Novel All-Optical Not Logic Based on Asymmetric SOA-Assisted Mach-Zehnder Interferometer

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Abstract

A novel scheme for all-optical NOT logic which exploits the cross-phase modulation (XPM) effect in an asymmetric SOA-assisted Mach-Zehnder Interferometer (SOA-MZI) has been proposed for the first time. Only two input beams are employed to achieve NOT operation in this new design. The scheme is validated and the system performance is optimized with various parameters through numerical simulations. This compact logic gate is helpful for future all-optical computing and networks.

Keywords: *All-optical logic device; All-optical NOT gate; Semiconductor optical amplifier; Mach-Zehnder interferometer, Contract ratio.*

1. Introduction

All-optical packet switching (OPS) networks are promising to satisfy the ever increasing bandwidth demand due to the continuously growing of Internet and multimedia service [1]. All-optical NOT logic operation has been addressed as a crucial element for future OPS networks, since it makes for a series of all-optical operations, such as address recognition, data encryption, and label swapping as well.

Hitherto, reported all-optical NOT logics include schemes utilizing SOA-assisted Sagnac interferometer [2], and NOT operations carried out by XOR using SOA-assisted Mach-Zehnder interferometers (MZI) [3], or ultrafast nonlinear interferometers (UNI) [4] etc. Among these designs, multi input signals (at least 3 input data) are required to fulfill the logic operation, which leads to a complex configuration and generates difficulty in practical applications. In this letter, we propose and analyze through numerical simulations a compact design based on an asymmetric SOA-assisted MZI scheme, which only need two input data to realize all-optical NOT logic. With scheme parameters optimized, result shows the new design could implement the logic function by yielding an output of more than 12dB in contrast ratio (CR) for 20Gb/s 2^{11}-1 PRBSs.

2. Principle and Modeling

As shown in Fig.1, the proposed logic consists of a symmetrical MZI with one SOA located in different relative position of each arm, , where SOA1 sits at the midpoint of the upper arm, and the position of SOA2 has an asymmetry distance from SOA1's, which generates a time delay of $\Delta\tau$ for light traveling. For the Boolean NOT calculation, the input clock signal A enters Port 1 and splits into two equal parts via Coupler OC1, named A1 and A2 respectively, acting as the probe signals. The input logic data B is amplified as the control signal and divided into two equivalent parts (B1 and B2) by Coupler OC2. When the control B is ONE, due to the XPM effect and the asymmetric location of the SOAs, a differential phase-shift is introduced to the probe signals in both arms of the MZI. If the phase-shift is controlled to around □, then the interferential output at port 4 is close to 0; In the case of B = ZERO, the SOA-MZI is balanced and no phase-shift between the two arms is generated, resulting in a pulse at the output. Therefore, all-optical NOT operation has been achieved.

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In analysis, signal A and B are synchronized in advance, and the SOAs are assumed to be identical and polarization- independent. Otherwise, the polarizations of both control signals traveling along the arms should be maintained the same. The loss and the amplified spontaneous emission (ASE) noise in SOAs are neglected for simplicity. Also, the group velocity dispersion is neglected since its effect on the pulse propagation is negligible along the SOA length.

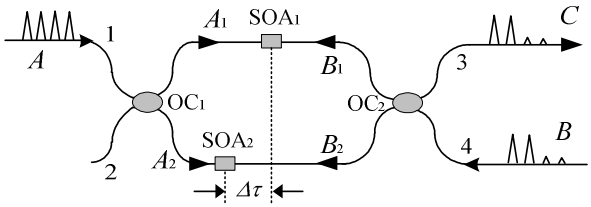

Figure 1. Configuration of all-optical NOT gate using SOA-MZI

Thereafter, taking into account the carrier pulsation effect and the nonlinear gain compression effect in SOA caused by carrier heating and spectral hole-burning, the SOA instant gain h(t) can be expressed as follows [5] [6]

$$\frac{dh(t)}{dt} = \frac{1}{1+\varepsilon \exp[h(t)]P(t)} \cdot \{\frac{h-h(t)}{\tau_c} - \varepsilon[\exp[h(t)]-1]\frac{dP(t)}{dt} - [\exp[h(t)]-1]P(t)(\frac{\varepsilon}{\tau_C} + \frac{1}{E_{sat}})\} \quad (1)$$

where $P(t)$ is the power of the input pulse, ε, τ_C, h_0 and E_{sat} are the nonlinear gain compression factor, the carrier lifetime, the small signal gain and the saturation energy of the SOA respectively. Considering the length effect of the SOA, the function of $G(t)$ and $h(t)$ can be formulated as follows [7]

$$h(t) = \frac{1}{L}\int_{-L/2}^{L/2} \ln G(t - 2\,zn_{SOA}/c)dz \quad (2)$$

where L, n_{SOA} are the length and the relative refractivity of SOA respectively, and c is the vacuum speed of light. Thereafter, the phase-shift of probe pulses in each arm, the switching window $T(t)$ and the output signal power P_{Out} of the logic gate at Port 3 are given by Equ.(4)~(6) respectively.

$$\Delta\phi_1(t) = -\alpha h(t)/2,\ \Delta\phi_2(t) = -\alpha h(t-\Delta\tau)/2 \quad (3)$$

$$T(t) = \frac{1}{4}\{G(t) + G(t-\Delta\tau) + 2\sqrt{G(t)G(t-\Delta\tau)}\cos(\Delta\phi_1(t) - \Delta\phi_2(t))\} \quad (4)$$

$$P_{Out}(t) = P_{In}(t)T(t) \quad (5)$$

Where $P_{In}(t)$ is the input power at Port1.

3. Simulations and Results

In simulations, a 250μm-length SOA is employed to provide a small-signal gain of 28dB. Both input logic signals are 20Gb/s RZ pulses pseudorandom bit sequences (PRBS) with a word length of 2^{11}-1. Except additional definition, the other default modeling parameters of the gate and characteristics of the data pulses and the probe pulses are: α = 5, ε = 0.4W^{-1}, refractive index of the SOA n = 3.62, $\Delta\tau$ = 2ps, extinction ratio of the data and probe signals ER_{data} = 30dB, wavelength of probe pulses λ_p = 1553nm, energy of the probe pulses E_p = 12.53fJ, energy of the data pulses E_{data}= 250fJ, pulsewidth full-width half-maximum (FWHM) of the pulses T_{Pulse} = 5ps, saturation energy E_{sat}=0.15pJ, carrier lifetime τ_c =80ps.

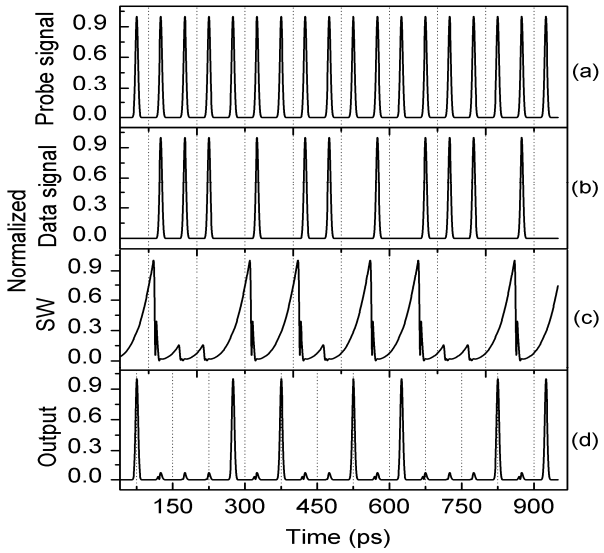

Figure 2. Simulation results of output signals for the NOT logic, (a) the input probe clock S1; (b) the input data S2, acting as control signals; (c) Switching window for the logic gate; (d) the output signal of NOT logic

Figure 2 shows the simulated logic performance for the NOT operation at 20G bit ratio, where (a), (b) accounts for the input control data *A* and the probe signal *B* respectively, (c) plots the switching window (SW) for bit operation, and (d) describes the NOT logic output. The NOT operation is realized with a *CR* of 10.8dB. In this case, *CR* is defined as the ratio of the minimum output peak power for ONE to the maximum output peak power for ZERO in dB unit, which is a key parameter to assess the performance of the logic gate. Since the parameters in the simulation are moderately selected, better performance can be expected by means of optimizing the parameters for SOAs and the delay time.

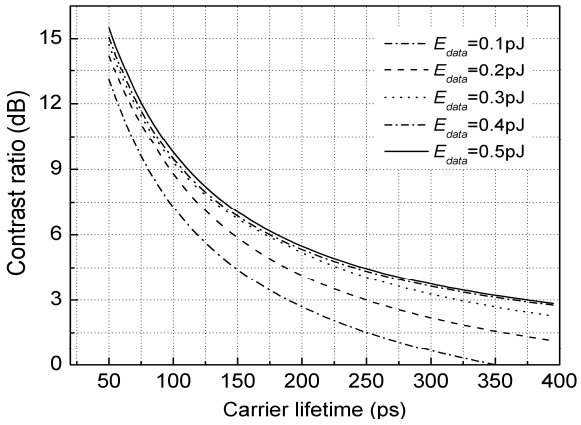

Figure 3. Output contrast ratio of the NOT gate against *t* and T_{Pulse}

Figure 3 plots the evolution of *CR* against the carrier lifetime τ_c of SOAs under different input pulse energy E_{data}. As can be seen in the fig., *CR* drops when τ_c increases for each E_{data} value. Since larger E_{data} is helpful to enhance the phase-shift between two arms of MZI, it is beneficial for higher *CR* output, which can be captured in the fig. However, *CR* could hardly rise further when E_{data} exceeds 0.4pJ, which indicates the SOAs are fully saturated and could not yield more phase-shift by only increasing the input pulse energy.

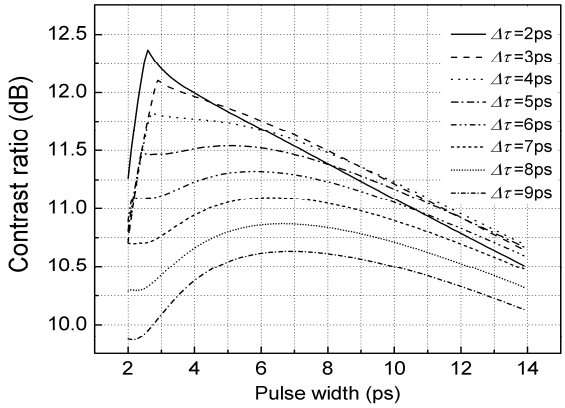

Figure 4. Output contrast ratio of the NOT gate as the functions of $\Delta\tau$ and T_{Pulse}

Figure4 shows the *CR* as a function of the input pulse width T_{Pulse} under different delay time $\Delta\tau$. For each $\Delta\tau$, *CR* rises with the increase of T_{Pulse}, and reaches a maximum value, then drops slightly, which indicates an optimum $\Delta\tau$ could be selected in system design for certain pulse width. In addition, *CR* degrades when $\Delta\tau$ increases generally, yet in situation of T_{Pulse} ≥7ps and $\Delta\tau$≤5ps, the difference in *CR* performance is negligible as shown in the fig. We can see when $\Delta\tau$≤6ps, T_{Pulse}≤14ps, the output *CR* exceeds 10.5dB, which is competent for practical applications.

4. Conclusion

We propose and demonstrate numerically a novel high-speed all-optical NOT gate based on SOA-MZI working at 20Gb/s. The contrast ratio of the logic output for the design has been analyzed and optimized by investigating the influence of input data and SOA-MZI's parameters. With design parameters optimally selected, the proposed design could implement the logic function by yielding an output of more than 12dB in contrast ratio for 20Gb/s 2^{11}-1 PRBSs. This logic gate provides a potential solution for future all-optical computing and networks.

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